

FIG. 1

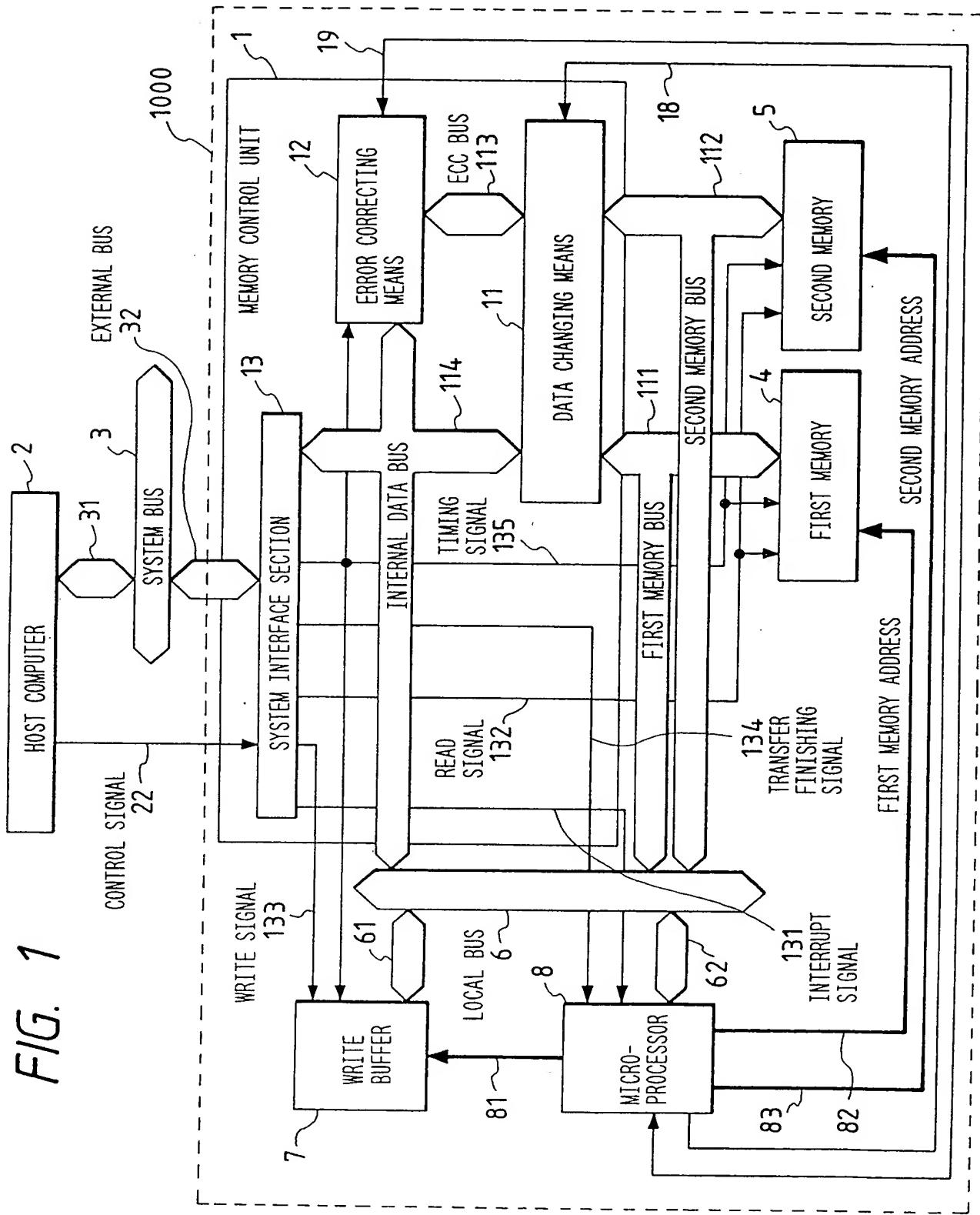


FIG. 2

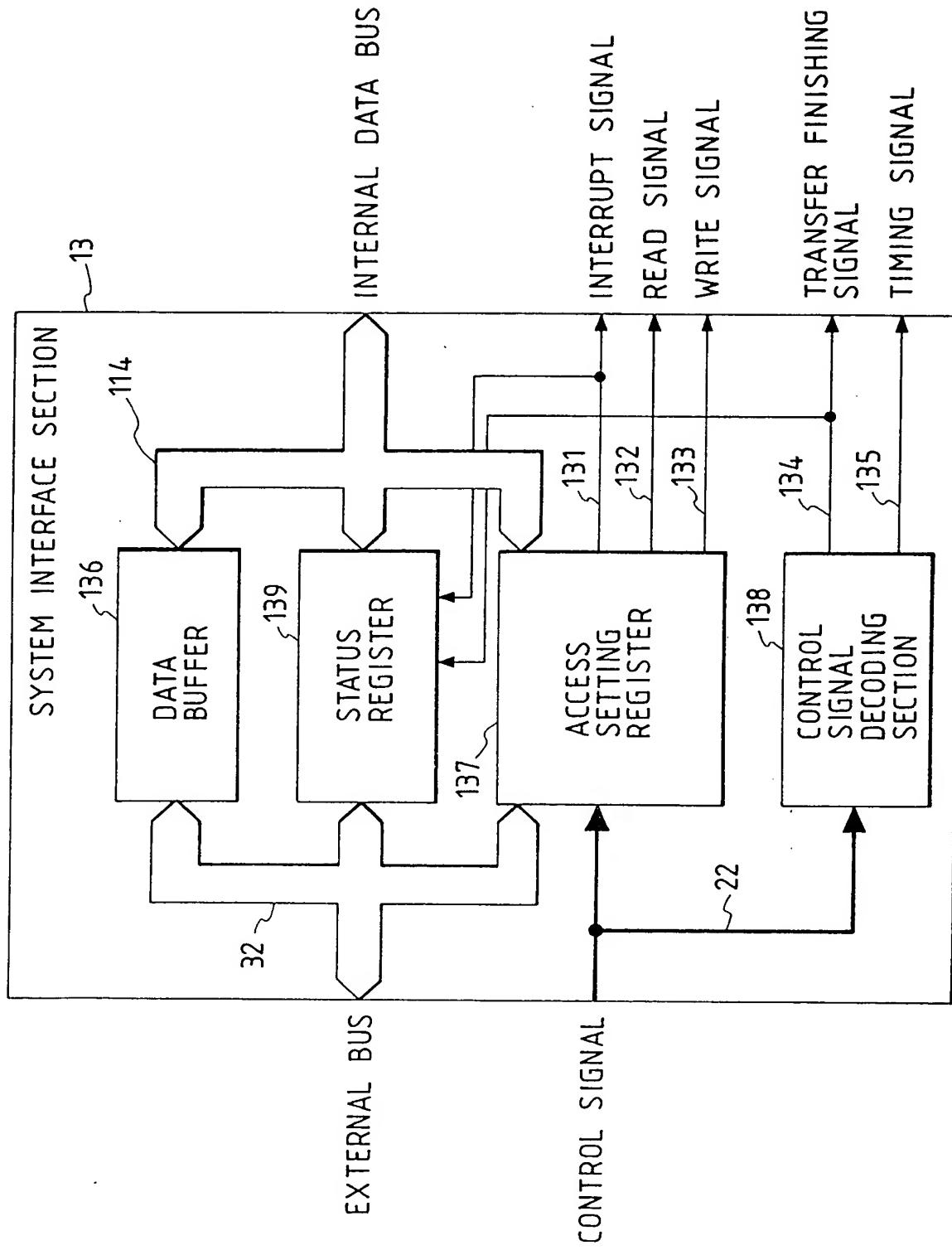


FIG. 3

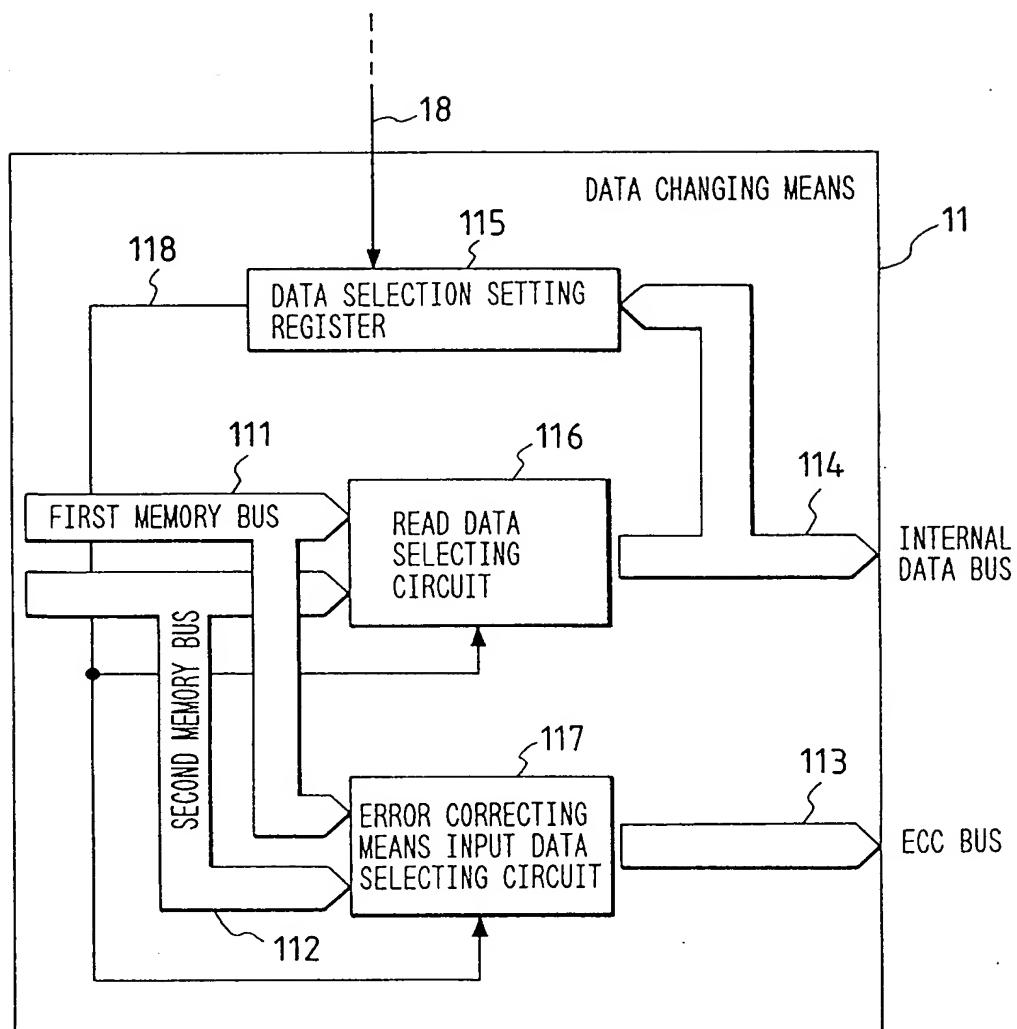


FIG. 4

(SELECTING CIRCUIT (116))

DATA SELECTION SETTING REGISTER 115	INTERNAL DATA BUS 114
0	FIRST MEMORY BUS 111
1	SECOND MEMORY BUS 112

FIG. 5

(SELECTING CIRCUIT (117))

DATA SELECTION SETTING REGISTER 115	EEC BUS 113
0	FIRST MEMORY BUS 112
1	SECOND MEMORY BUS 111

FIG. 6

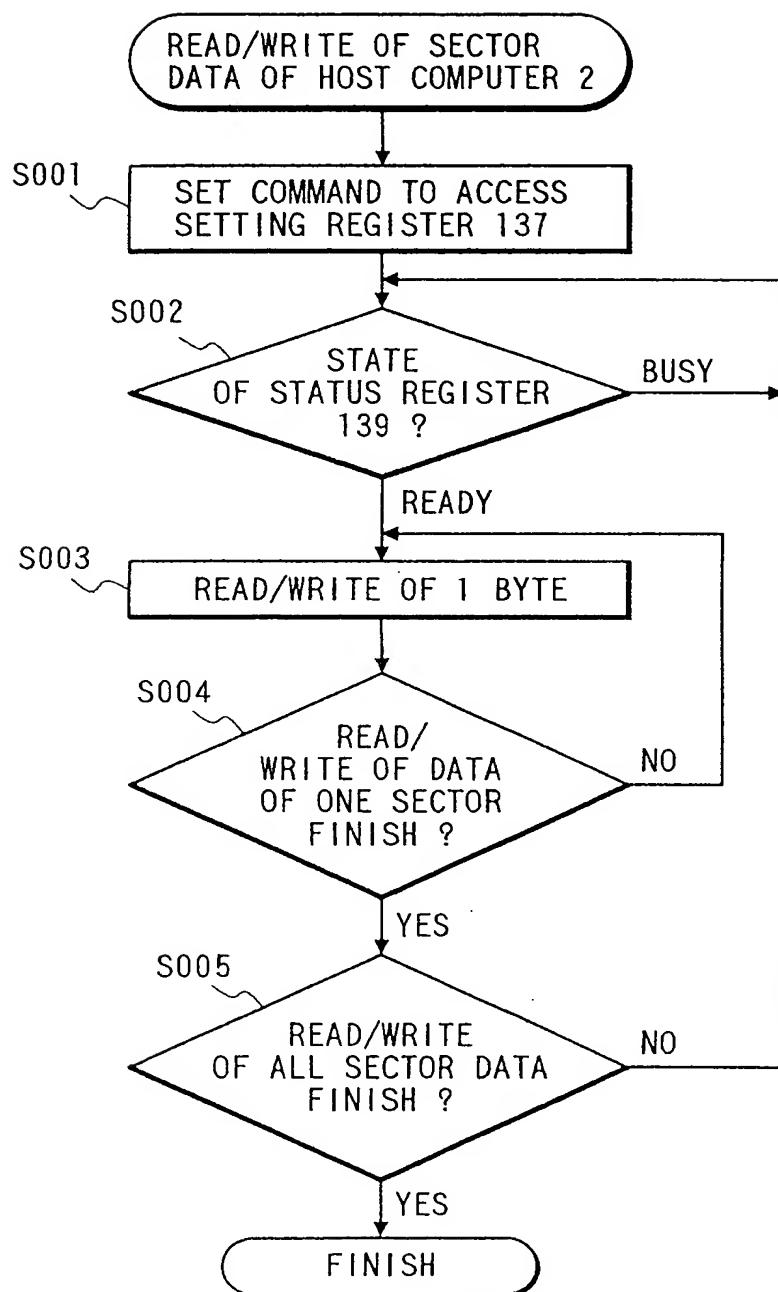


FIG. 7

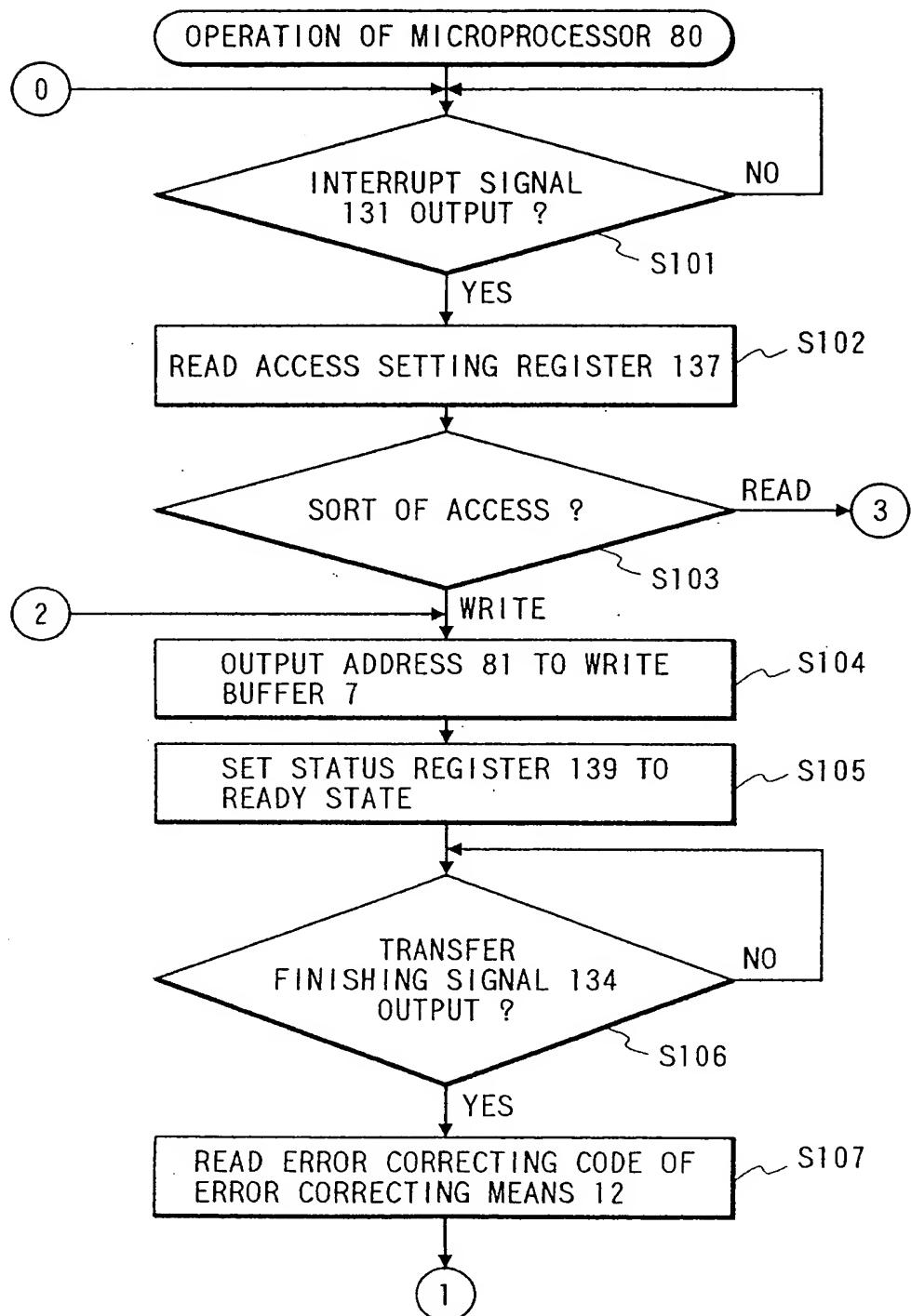


FIG. 8

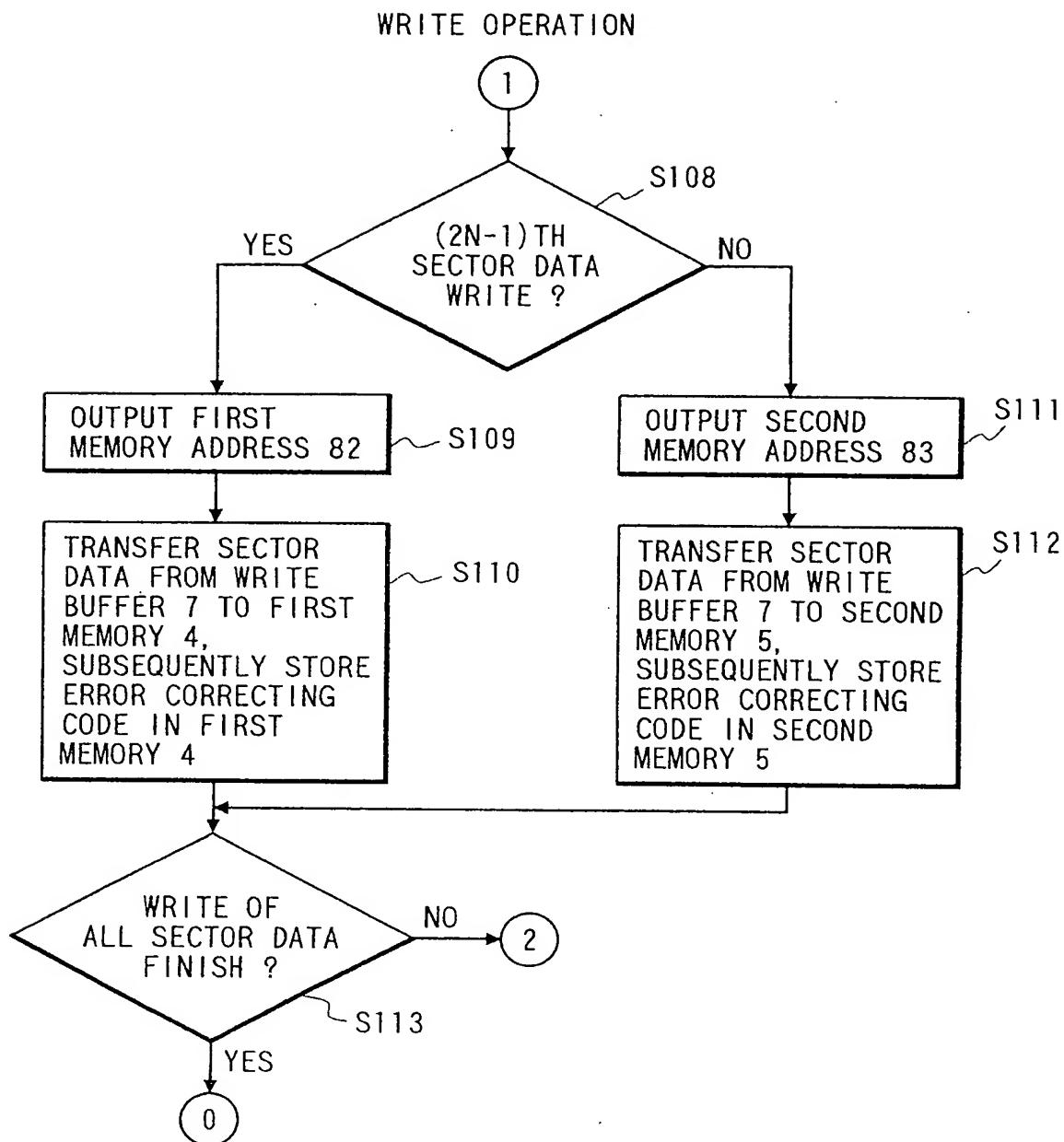


FIG. 9

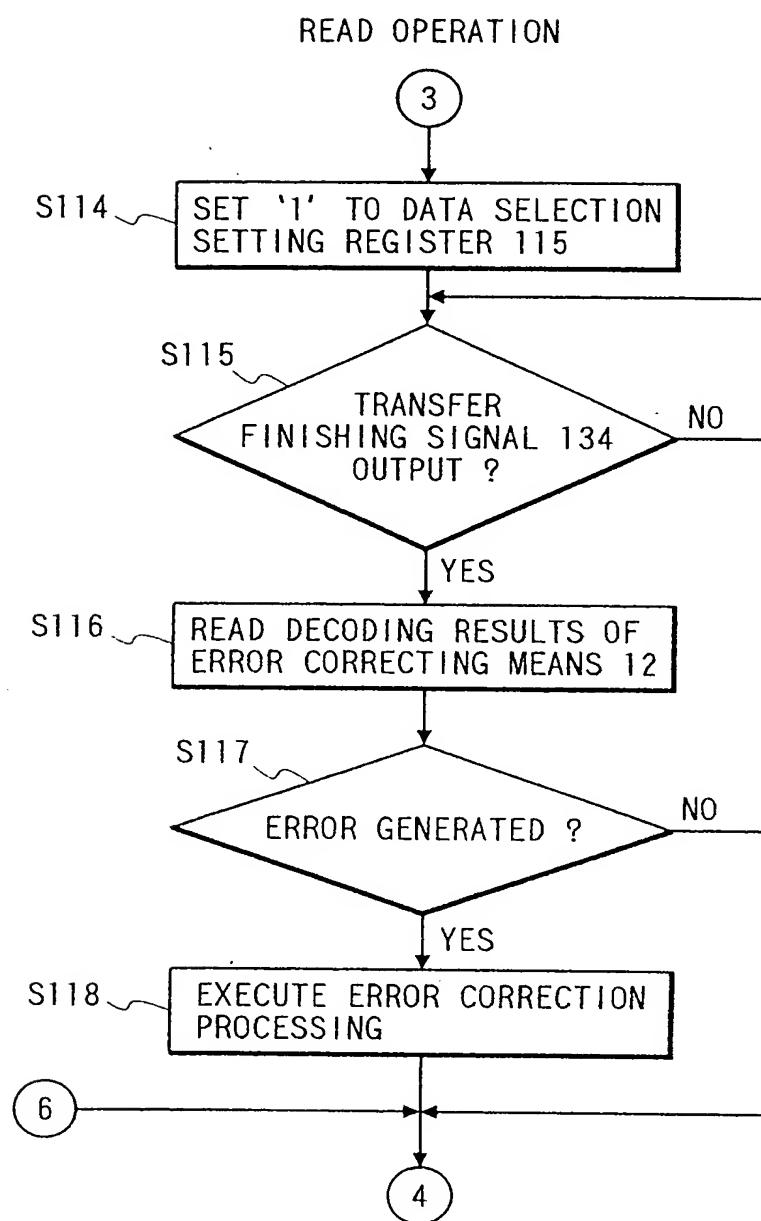


FIG. 10

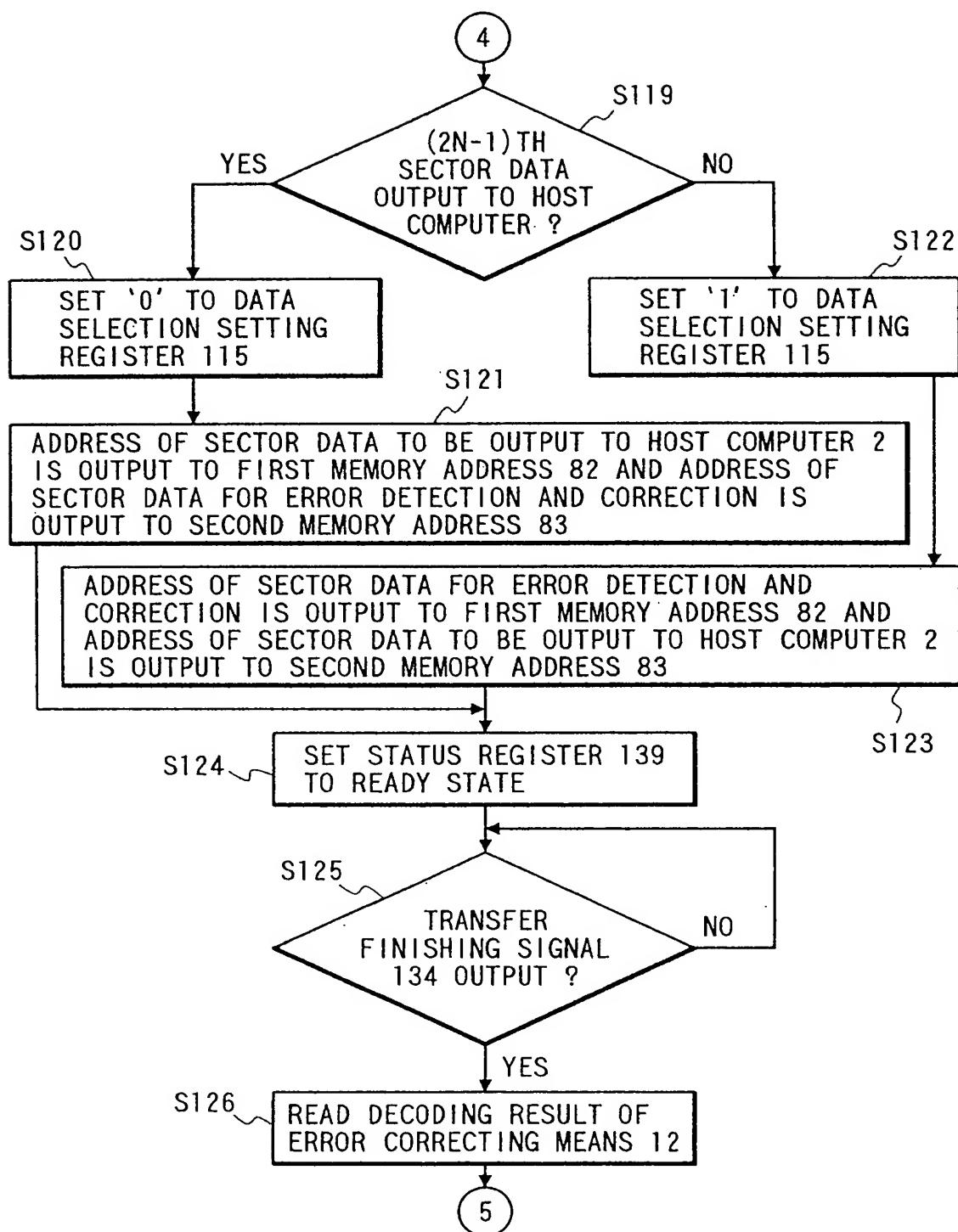


FIG. 11

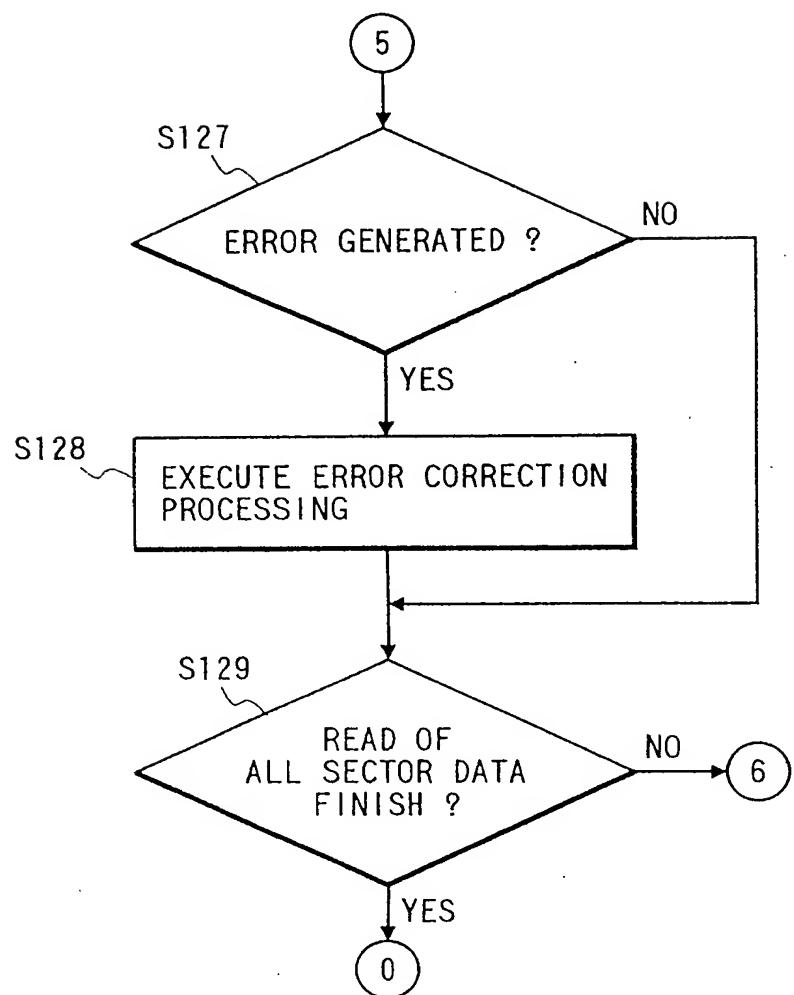


FIG. 12

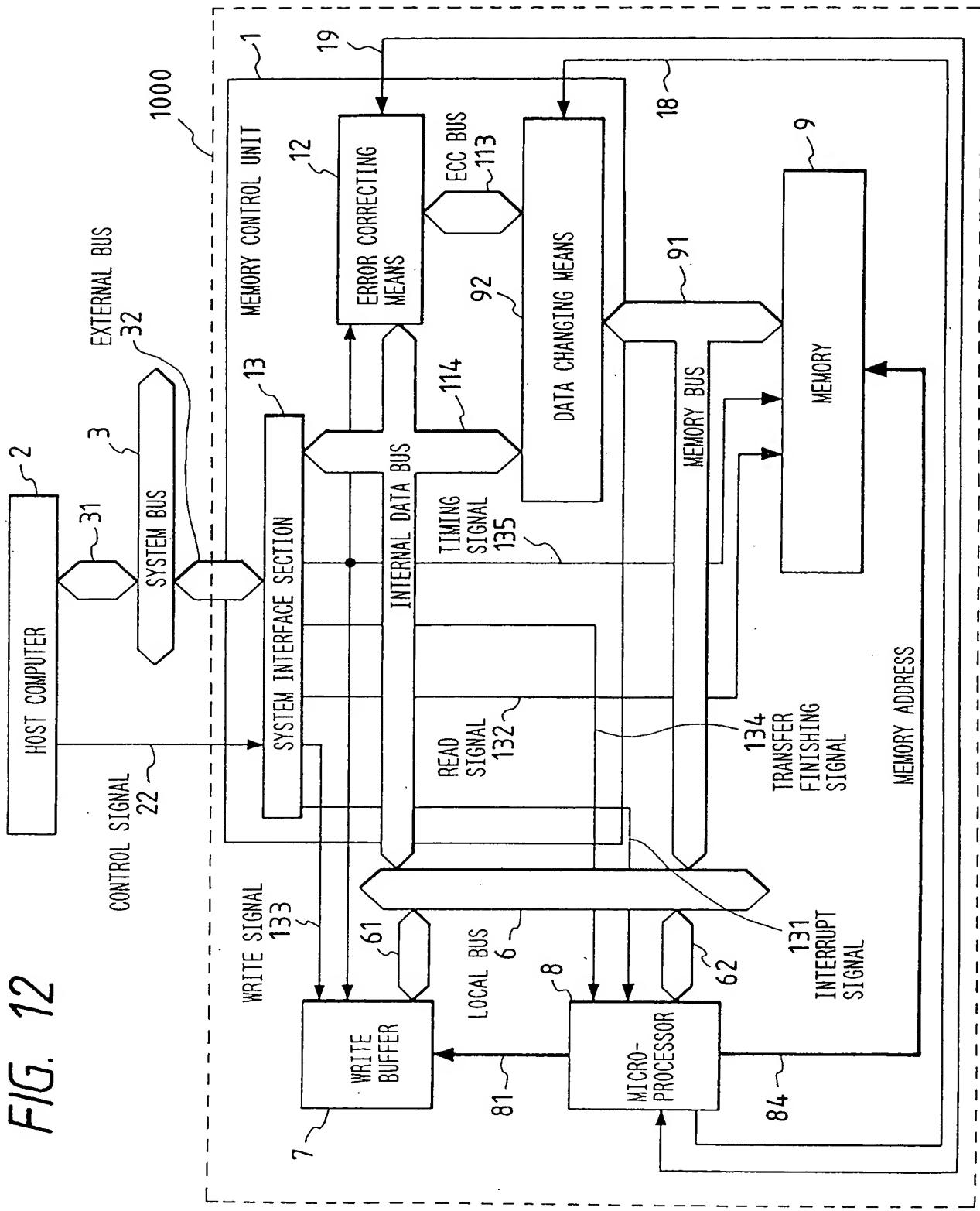


FIG. 13

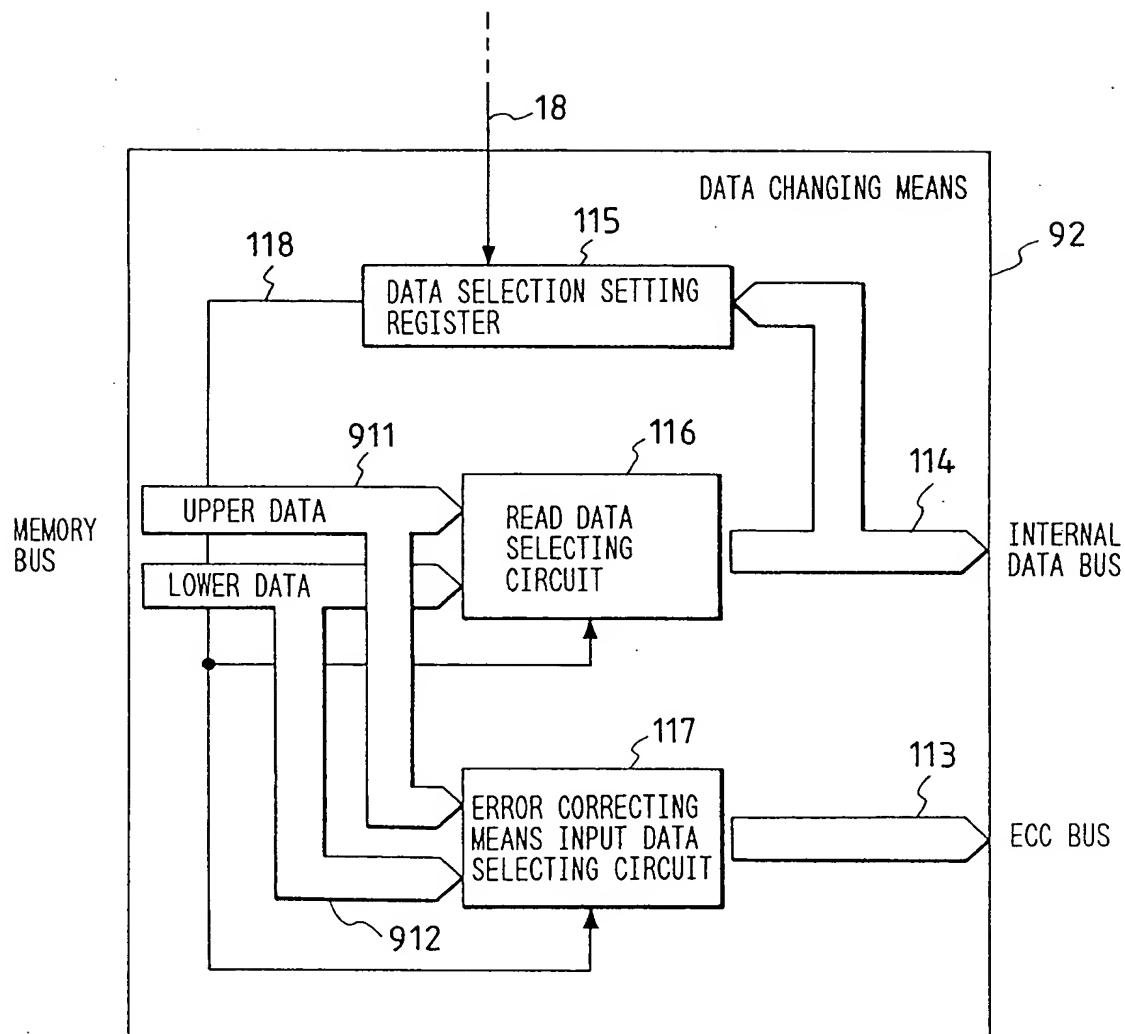


FIG. 14

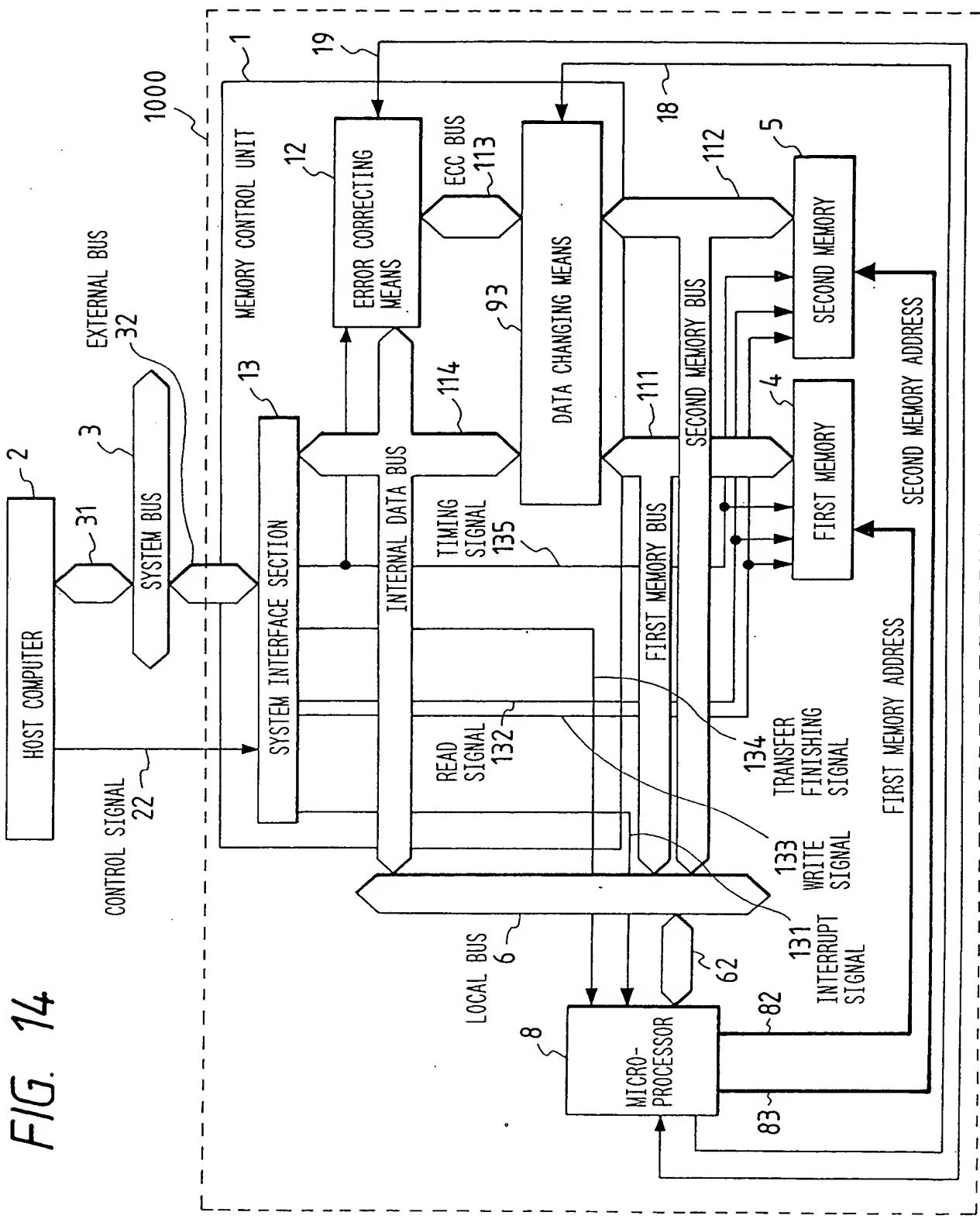


FIG. 15

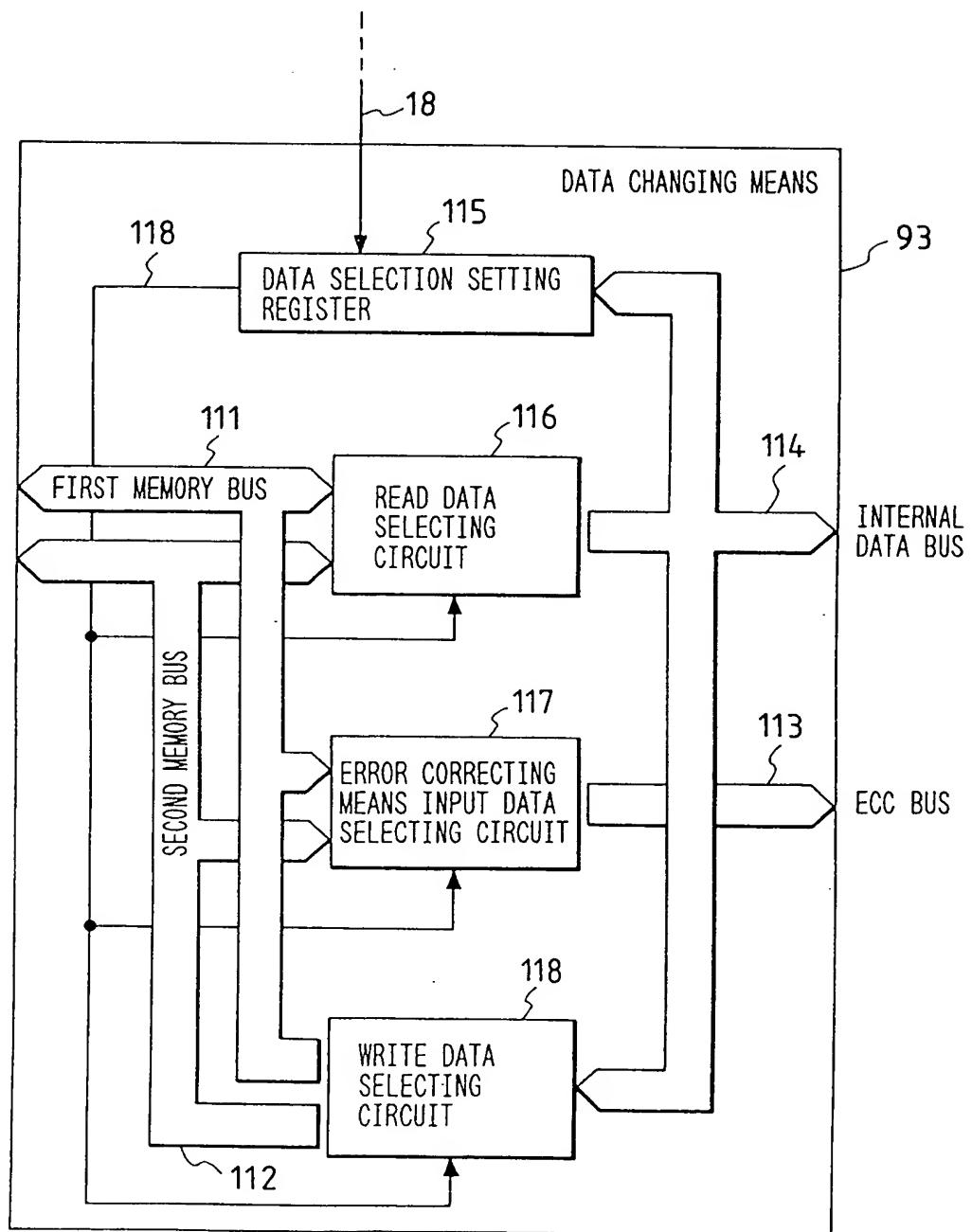


FIG. 16

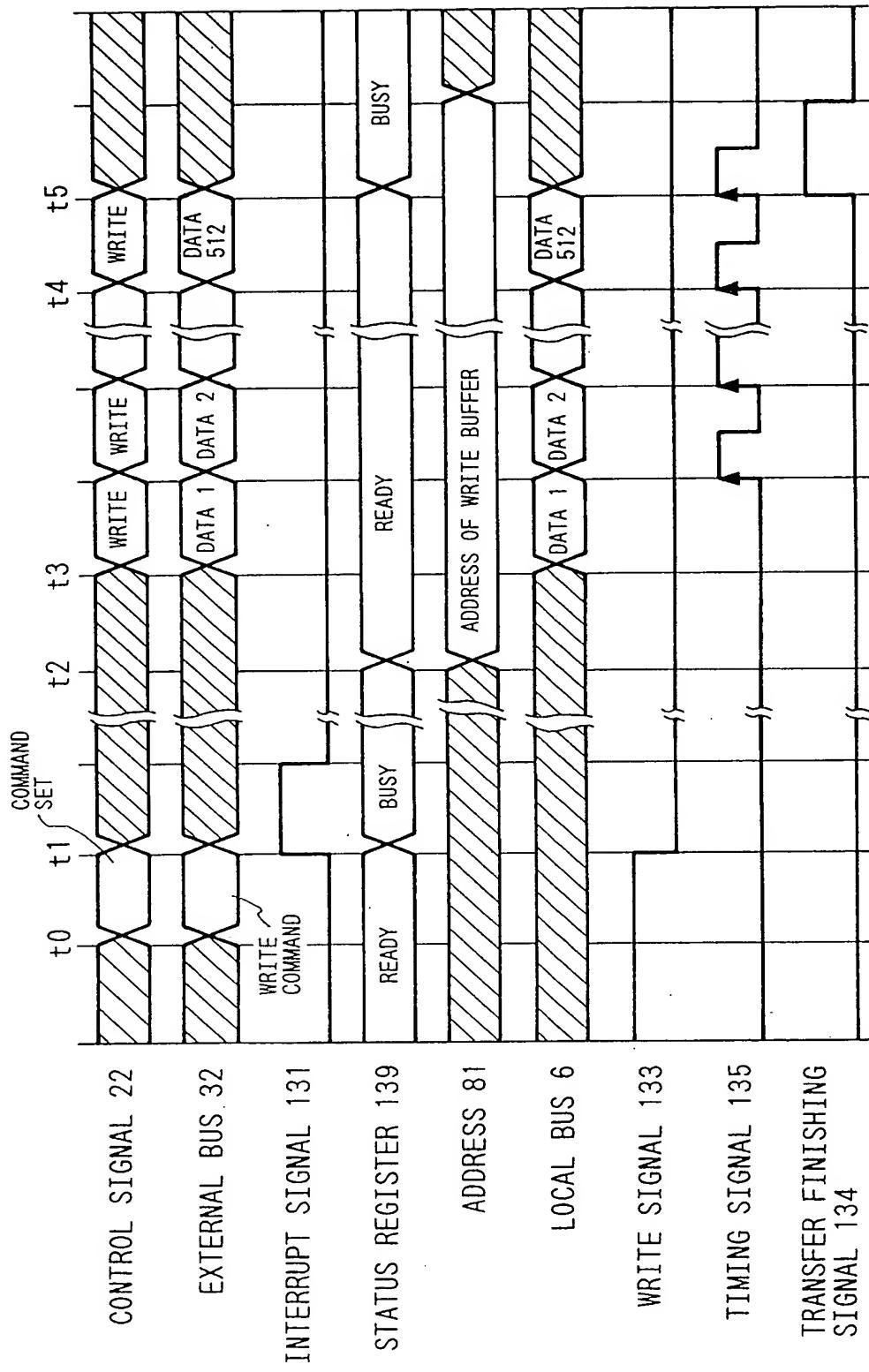


FIG. 17

FIRST MEMORY 4		SECOND MEMORY 5	
ADDRESS	CODE	ADDRESS	CODE
100	DATA 1-1	DATA 1-2	-----
			DATA 1-512
102	DATA 3-1	DATA 3-2	-----
			DATA 3-512
			CODE 3-1
			CODE 3-2
			CODE 3-3
			1ST SECTOR DATA
			3RD SECTOR DATA

FIRST MEMORY 4		SECOND MEMORY 5	
ADDRESS	CODE	ADDRESS	CODE
101	DATA 2-1	DATA 2-2	-----
			DATA 2-512
103	DATA 4-1	DATA 4-2	-----
			DATA 4-512
			CODE 4-1
			CODE 4-2
			CODE 4-3
			2ND SECTOR DATA
			4TH SECTOR DATA

FIG. 18

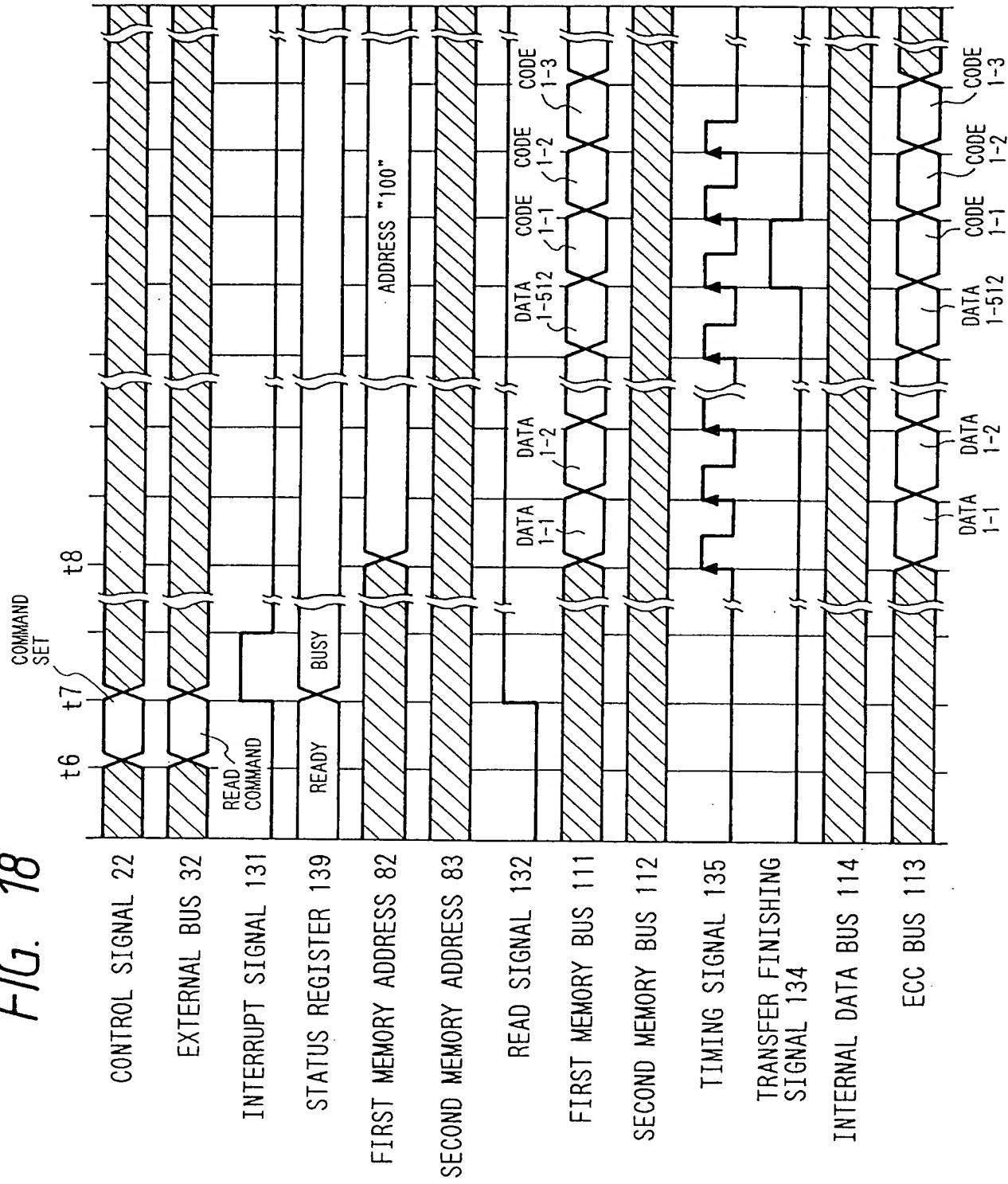


FIG. 19

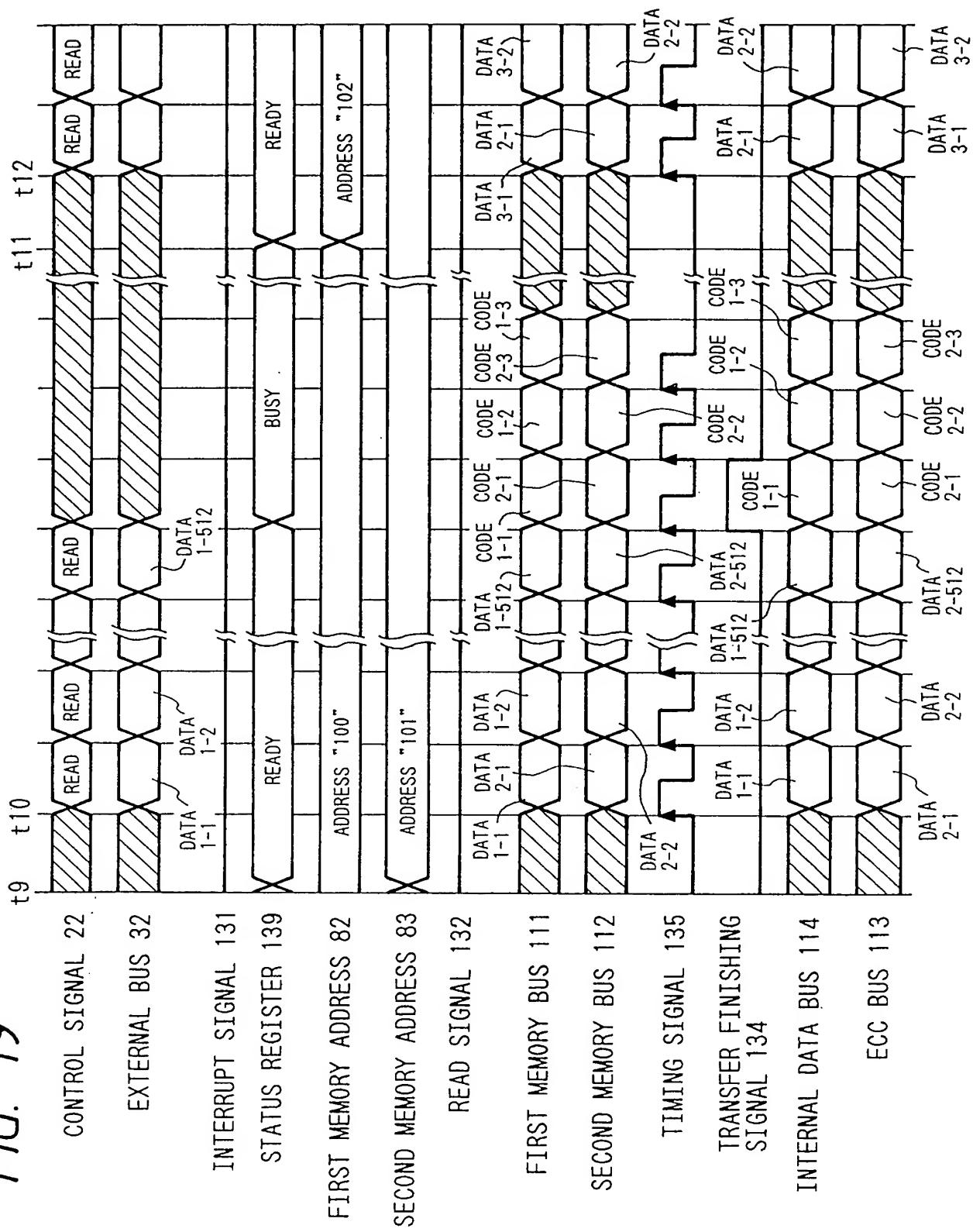


FIG. 20

